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A u.h.f. field-strength measuring receiver with digital display

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RESEARCH DEPARTMENT

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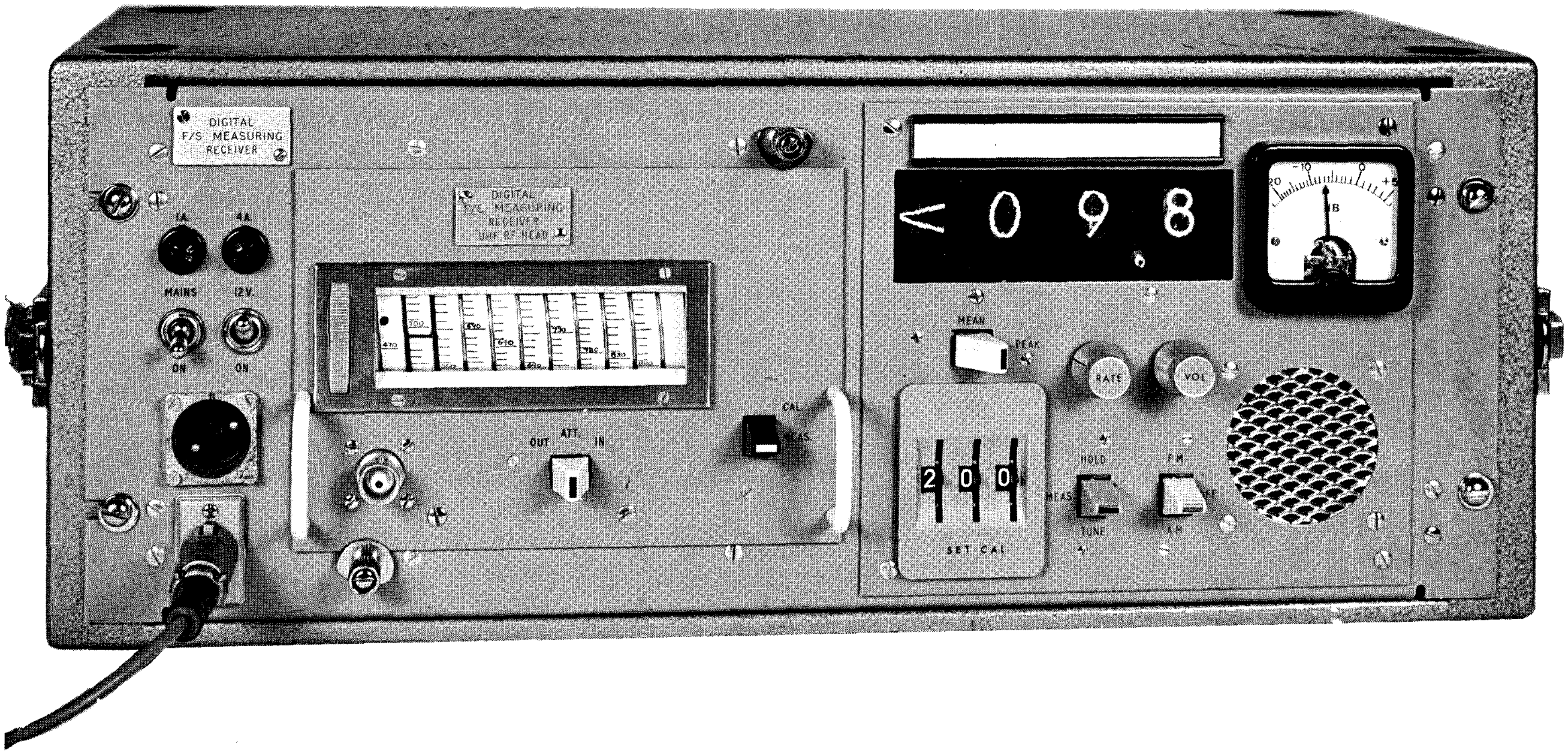

Fig. 1 - Photograph of digital receiver

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A U.H.F. FIELD-STRENGTH MEASURING RECEIVER WITH DIGITAL DISPLAY

SUMMARY

This report describes a receiver which has been designed to measure the field strength within the service area of television transmissions in the frequency range 470 to 890 MHz.

For ease of operation and to reduce operational errors, the measured field strength is displayed directly in decibels relative to 1 μV/m on numeral indicators. Either sound or vision transmissions may be measured, the vision measurement being that of the peak of the synchronizing pulse.

A loudspeaker is provided for identifying transmissions and a semiconductor noise diode is included for checking the calibration of the receiver. The equipment can be operated from either a mains supply of 200 to 250 V, 50 Hz or a vehicle 12 V battery with negative earth.

Most of the active devices in the receiver are integrated circuits.

1. INTRODUCTION

With the expansion of the u.h.f. television service, the need has arisen for tunable receivers capable of measuring the field strength within the service areas. It was in order to meet this demand for measuring equipment that the receiver described in this report was developed.

The receiver consists of a standard commercial u.h.f. tuner followed by an intermediate frequency (i.f.) amplifier containing electronically operated attenuators. These are adjusted automatically in steps of 0·2 dB until the detector output reaches a standard level. These steps are counted and presented as a digital display of field strength in decibel units. The attenuator has a range of 70·2 dB and this may be extended by the use of a built-in 20 dB radio frequency (r.f.) attenuator. A photograph of the receiver is shown in Fig. 1.

2. METHOD OF OPERATION

The method of operation can be followed from the block schematic of Fig. 2. The single-shot 1 Hz oscillator starts and at the end of the cycle sends a pulse to both the i.f. and display counters thereby resetting them to zero. This sets the i.f. attenuation to its maximum value. A delayed pulse from the 1 Hz oscillator then triggers a monostable which sends a pulse to the decade switch and to a bistable. The decade switch (set during aerial calibration) puts an initial count into the display counter so that the final display is in field strength in decibels relative to 1 μV/m. Theoretically the setting of the decade switch represents the calibration factor[1] whereby microvolts at the aerial terminal are converted into microvolts/metre.

The bistable starts the 700 Hz oscillator which sends pulses to both the i.f. and display counters. The i.f. counter removes an attenuation step of 0·2 dB for each pulse from the 700 Hz oscillator and the display counter, being operated in parallel with the i.f. counter, counts the number of steps. When the detector output reaches a predetermined level, the bistable is returned to its original state thereby stopping the 700 Hz oscillator. This opens the store and transfers the count from the display counter to the store. The count from the store is then decoded and displayed during the next cycle of the 1 Hz rate oscillator. The resetting of the bistable also retriggers the 1 Hz oscillator to repeat the operation.

If the incoming signal is outside the measurement range of the receiver, gates operate to stop the counter and a character tube is lit in the display to give either a + sign for too high a signal or a < sign for too low a signal. A further refinement is the reduction of the 700 Hz oscillator to approximately 7 Hz as the detector output approaches the predetermined level. This ensures that the detector has time to reach its peak value.

In an alternative method of operation, the i.f. attenuators can be locked and then the output of the detector drives a meter. This provides a fixed-gain receiver with a linear voltage response that may be used for observing fading and for obtaining the mean reading for a standing-wave pattern. The meter scale is shaped by diodes so that an approximately linear decibel scale is obtained over a range of +5 to −20 dB relative to the fixed display. This method of operation is also used for tuning and identifying the signal on the loudspeaker.

A peak detector is provided for the measurement of vision signals so that the field strength displayed is directly related to the peak transmitter power and is independent of picture content.

A semiconductor noise diode[2,3] is used for checking the calibration of the receiver. The r.f. head is designed as a plug-in unit so that it will be possible to develop heads for other bands should the need arise.

Stabilized power supplies are used throughout so that the receiver may be operated from 200 V to 250 V 50 Hz mains or from a 17 V to 10 V vehicle battery with negative earth. A diode prevents damage should a battery of wrong polarity be inadvertently connected to the receiver.

3. CALIBRATION

Any field strength measuring receiver requires two types of calibration, one in absolute terms at infrequent intervals and the other a more frequent check during field use to see that factors affecting the short term calibration are compensated. These more frequent checks are performed using an internal calibrator unit employing a semiconductor noise diode as already mentioned.

For any one frequency the absolute calibration is possible in two ways. The receiver may be calibrated in terms of the voltage at the input and a factor, based on the frequency, aerial gain and feeder loss, applied to convert the input e.m.f. to field strength. Alternately the complete equipment may be calibrated in a standard field. In practice it is advisable to perform both calibrations in order to eliminate any errors due to aerial and feeder faults.

The latter calibration is achieved by placing the whole receiving system, including the aerial and feeder, in a known field and then adjusting the decade switch to produce this value of field on the digital display. The noise-diode calibrator is then switched on and the reading of the digital display noted. This procedure is repeated for several known fields and the average of the calibrator readings on the digital

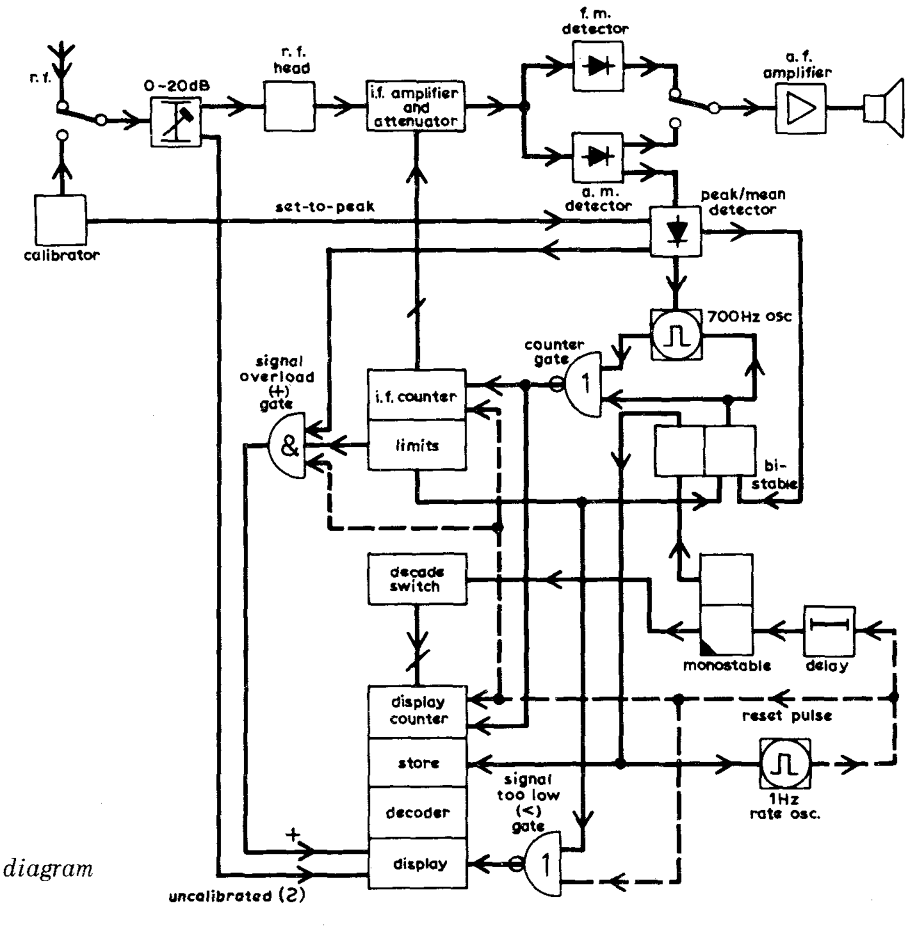

Fig. 2 - U.H.F. digital receiver block diagram

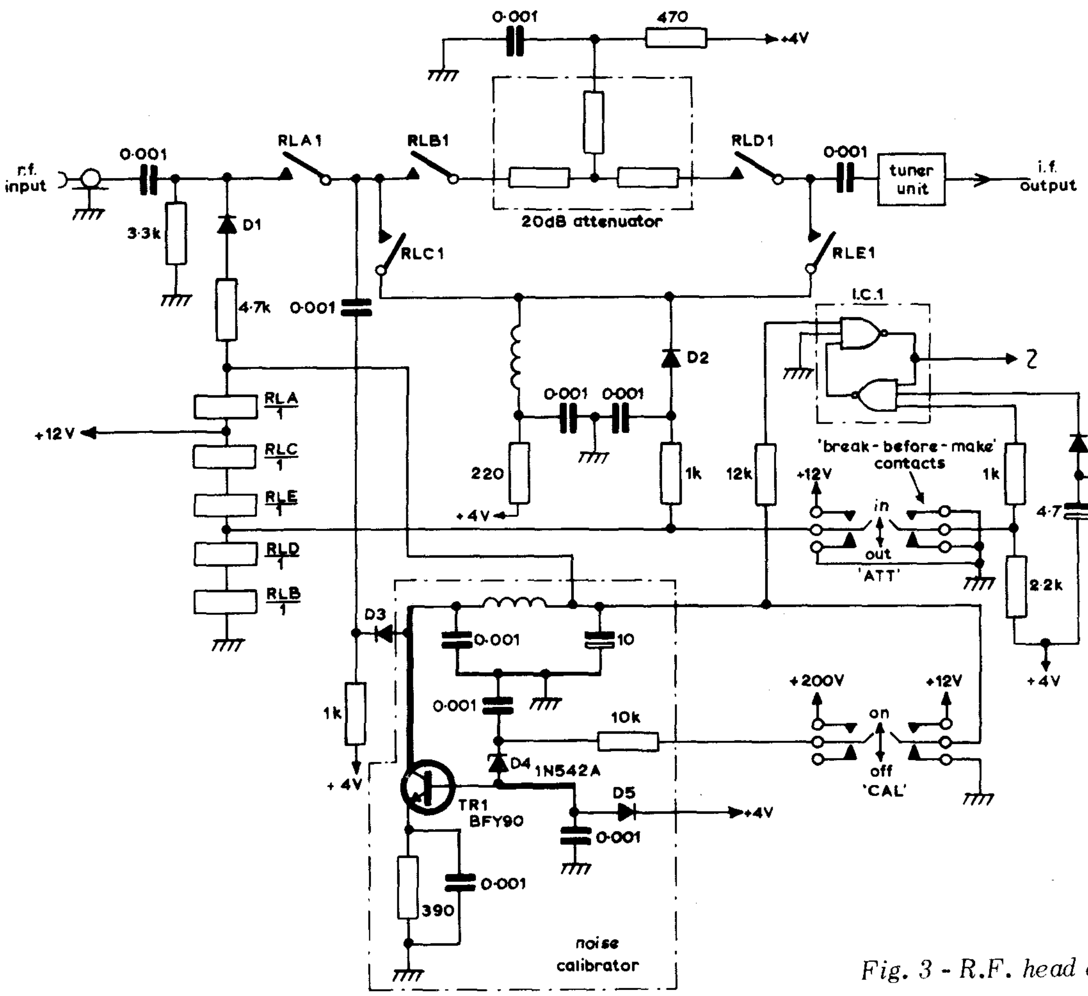

Fig. 3 - R.F. head circuit diagram

display taken. The figure so obtained should be within ± 1 dB of the calculated value obtained earlier. If it is outside this range an error is indicated which is corrected before the receiver leaves base.

The short term calibration is dependent upon the stability with time of both the passband of the receiver and the output level of the noise-diode calibrator. The latter has been shown[2] to be better than ± 0·25 dB over a period of several months while careful design ensures the stability of the former. In the field the noise diode is switched on and the digital display compared with the absolute value obtained earlier for the particular frequency in use. Any small variations can be taken up by adjustment of the decade switch.

4. SPECIFICATION OF THE RECEIVER

(1) Frequency Range : Continuously tunable over the range 470 to 860 MHz.

(2) Input Impedance : 50 ohms, unbalanced.

(3) Bandwidth:

Frequency relative to mid-band frequency	Attenuation relative to that at mid-band
± 130 kHz	– 3 dB
±1500 kHz	–60 dB

(4) Spurious Responses :

Image frequency rejection	>50 dB
i.f. rejection	>60 dB

(5) Intermediate Frequency : 37·0 MHz.

(6) Signal Strength Range : From 30 μV to 1 V e.m.f. at the receiver input.

(7) Accuracy : ± 1 dB

(8) Display :

(a) Digital display with facility for reading in decibels relative to 1 μV/m and indication when signal is outside measurement range of receiver.

(b) Meter display of +5 dB to –20 dB relative to the digital display when the i.f. attenuators are locked.

(9) Audio Output : Loudspeaker driven from either a.m. or f.m. detectors.

(10) Calibrator : Wideband u.h.f. noise calibrator.

(11) Temperature Range : The performance of the receiver to be satisfactory over a temperature range of 0° to +45°C.

(12) Power Supplies : Either 200 to 250 V 50 Hz or 12 V battery with negative earth. Power consumption 30 W approx.

(13) Dimensions : The receiver to be housed in an aluminium case measuring 530 x 330 x 200 mm.

(14) Weight : 10·5 kg.

5. CIRCUIT DESCRIPTION

5.1. The R.F. Head

The r.f. head as shown in Fig. 3 consists of a commercial u.h.f. television tuner together with a r.f. attenuator and noise calibrator.

The tuner is unmodified apart from a slight re-adjustment of the local oscillator and output circuits to enable the head to cover the frequency range with an i.f. of 37 MHz. A drum tuning control is used to give a total scale length of 1·2 m. Since the scale is substantially linear, this enables the frequency to be easily set.

Between the aerial socket and the r.f. tuner there is a 20 dB attenuator which is switched in or out of circuit as required by reed relays. These relays and their associated connectors are designed as coaxial lines to keep a good impedance match, eliminate direct pick-up and to act as an impedance transformer from 50 to 75 ohms. In the 'attenuate' condition, the direct path link is also short-circuited to earth at r.f. by a heavily conducting diode D2 to reduce breakthrough.

The calibrator consists of a semiconductor diode D4 operated in a reverse breakdown condition at 8 mA where it gives a high, stable level of noise. This is followed by a wideband amplifier TR1. The overall noise level is approximately 58 dB above thermal and is constant to within ± 1 dB over the range 470 to 890 MHz and better than this with time. When the calibrator is switched on the aerial socket is disconnected from the attenuator by a relay RLA and short-circuited to ground by a conducting diode D1. A diode D3 connects the noise calibrator to the attenuator.

Two three-input gates of integrated circuit IC 1 in Fig. 3 are interconnected to form a bistable which operates the 'uncalibrated' sign on the display. This appears whenever the attenuator switch is operated and warns the operator that the receiver constants have been changed. This sign is also displayed when the receiver is initially switched on. Operation of the calibrator resets the bistable and clears the 'uncalibrated' sign.

5.2. The Intermediate Frequency Amplifier

The i.f. amplifier unit consists of four main sections:–

(a) An input filter to define the overall bandwidth.
(b) A four-stage amplifier with electronically switched attenuators.
(c) Detectors for a.m., f.m., peak and mean.
(d) A counter with drive oscillator and controlling logic.

5.2.1. The Input Filter

The input filter uses a four-section bandpass circuit with notch sections above and below the pass-band to improve the overall response.

5.2.2. I.F. Amplifier with Attenuators

The basic i.f. amplifier stage uses an integrated circuit and is shown in simplified form in Fig. 4. The

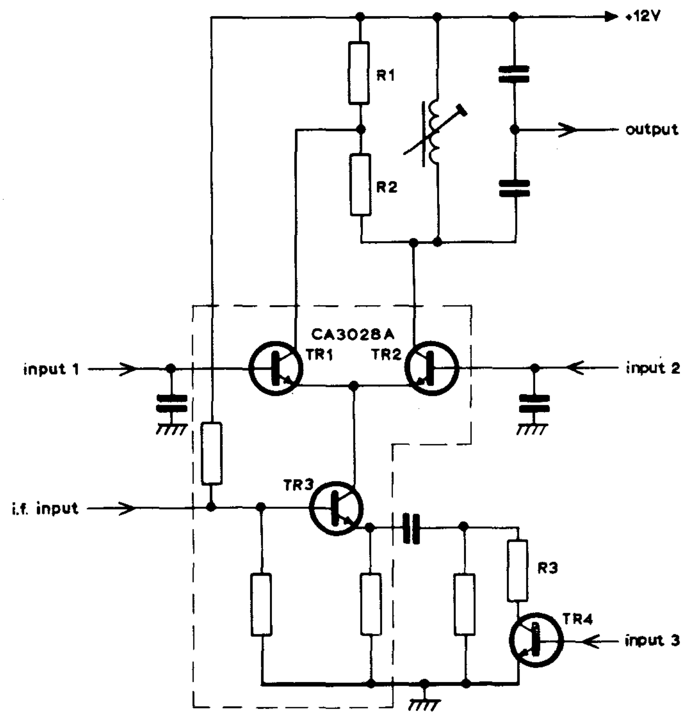

Fig. 4 - I.F. amplifier stage simplified circuit diagram

circuit is connected as a cascode amplifier using either transistors TR1 and TR3 or TR2 and TR3. The i.f. counter (see 5.2.4.) drives the base circuits of TR1 and TR2 so that only one of the two transistors is conducting. When TR2 is conducting the stage will have a high gain but if TR1 is conducting the current gain will be the same at the collector but resistors R1 and R2 act as a universal shunt and reduce the output in the ratio of

$$\frac{R1}{R1 + R2}$$

By correct choice of R1 and R2 attenuations of 6·4, 12·8 or 25·6 dB may be obtained. In practice, some slight adjustment of the resistor values is required to compensate for changes in output resistance of the integrated circuit.

Small step changes of attenuation are made by varying the emitter feedback of the transistor TR3. This is achieved by shunting R3 across the emitter resistor by switching TR4 into conduction.

In the four i.f. amplifier stages the first has attenuators of 25·6 and 3·2 dB, the second 25·6 and 1·6 dB, the third 12·8 and 0·8 dB whilst the final stage has 6·4, 0·4 and 0·2 dB, both the small steps being shunts on the emitter resistor. A typical i.f. amplifier passband is shown in Fig. 5.

5.2.3. The Detectors

The detectors and metering circuit are shown in Fig. 6. The final stage of the i.f. amplifier feeds a limiter and discriminator for f.m. signals and the

simple detector D1 which supplies the peak/mean detector, metering circuit and the a.m. output to the audio amplifier.

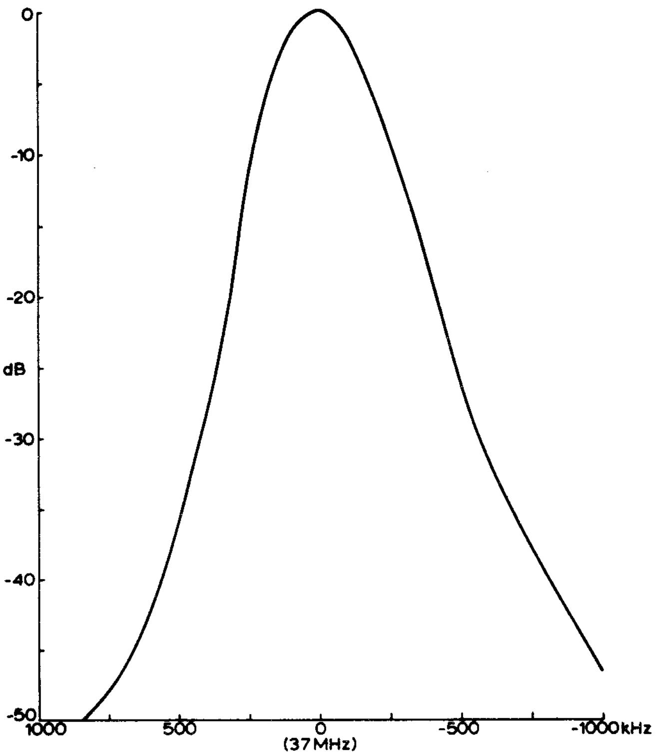

Fig. 5 - Overall response of i.f. amplifier

The peak detector[4] uses an integrated circuit operational amplifier IC 1 with its positive-going and negative-going negative feedback paths isolated by diodes D2 and D3. The positive-going diode output is used to charge a capacitor C1 very rapidly and when the signal falls the diode D2 opens leaving C1 to discharge slowly through R1. During peak measurements R2 is short-circuited by TR1 which is conducting heavily.

For mean measurements, TR1 is cut off and effectively inserts R2 in the charging circuit of C1 so that a mean voltage now appears across C1. TR13 is a clamp on the capacitor C1 to ensure that it is fully discharged at the end of each measurement. The voltage across the capacitor C1 supplies a compound emitter follower (TR8, TR9) which has three associated circuits. The first (TR10 to TR12) slows the count oscillator as the standard level is approached. The second (TR14) stops the 700 Hz oscillator when the detector output reaches the standard level, and the third gives the overload indication via the diode logic D7 to D10.

The detector circuit is biased by the 4 V supply and the collector potential of TR9 for zero input signal is about 3·1 V. When this rises to about 4·4 V TR10 will start to conduct causing TR11 to conduct heavily and cut off TR12. This effectively inserts R3 into the timing circuit of the 700 Hz oscillator (I.C.14, Fig. 7) thereby reducing its frequency and the stepping rate of the attenuators to about 7 Hz. When the output from TR9 reaches 5·3 V TR14 will start to conduct. This will reset the bistable (IC 6 Fig. 7) and stop the 700 Hz oscillator.

5.2.4. The I.F. Counter and Associated Logic

The attenuators in the i.f. unit are driven from a counter which is basically a nine-stage binary counter. The last two stages are interconnected to form a divide-by-three stage so that two attenuation steps of 25·6 dB can be used, as mentioned in Section 5.2.2. The reason for a divide-by-three stage is because three states are required namely none, one or both stages of 25·6 dB. If a binary stage had been used an attenuator of 51·2 dB would have been required and this would be difficult to make.

The high-value attenuators (>6·4 dB) are driven from pairs of amplifiers which also set the output swing at 7 V or 4 V. The logic circuits associated with the i.f. amplifier are shown in Fig. 7. Multiple gates IC 2 and IC 10, connected to the i.f. counter, detect whenever maximum or minimum values of attenuation are reached so that warning of limiting values can be given.

At the start of a measuring cycle a pulse from the rate oscillator TR16 is used to reset the i.f. counter to zero and the attenuators to maximum. It also triggers the monostable IC 4 via a resistance-capacitance delay and amplifier IC 3. The pulse from the monostable is inverted by IC 5 and fed into the decade switch for setting the display counter (Section 5.3) to its initial value. The trailing edge of the monostable pulse operates the bistable IC 6 which in turn permits the 700 Hz oscillator IC 14 to start. The output of the oscillator passes via the counter gate IC 7 to the i.f. counter and also to the display counter via the inverting amplifier IC 12. The 700 Hz oscillator continues to run until the bistable is reset by either the detector reaching the standard level or the counter reaching maximum count. The resetting of the bistable also supplies a resetting pulse via the delays IC 9 and IC 13 to the display stores which then take up the count from the display counter.

If the maximum i.f. gain is reached before the standard output is obtained from the detector, the coincidence gates IC 10 produce an output which resets the bistable and stops the count. At the same time a second bistable IC 8 is set and this produces a < sign on the display, indicating that the input signal is too small to measure. This sign is cleared by the resetting of the first bistable IC 6 when a signal is again present at the detector.

If on the other hand too strong a signal is being received, the initial detector output will be above standard level; the bistable is then held so that the

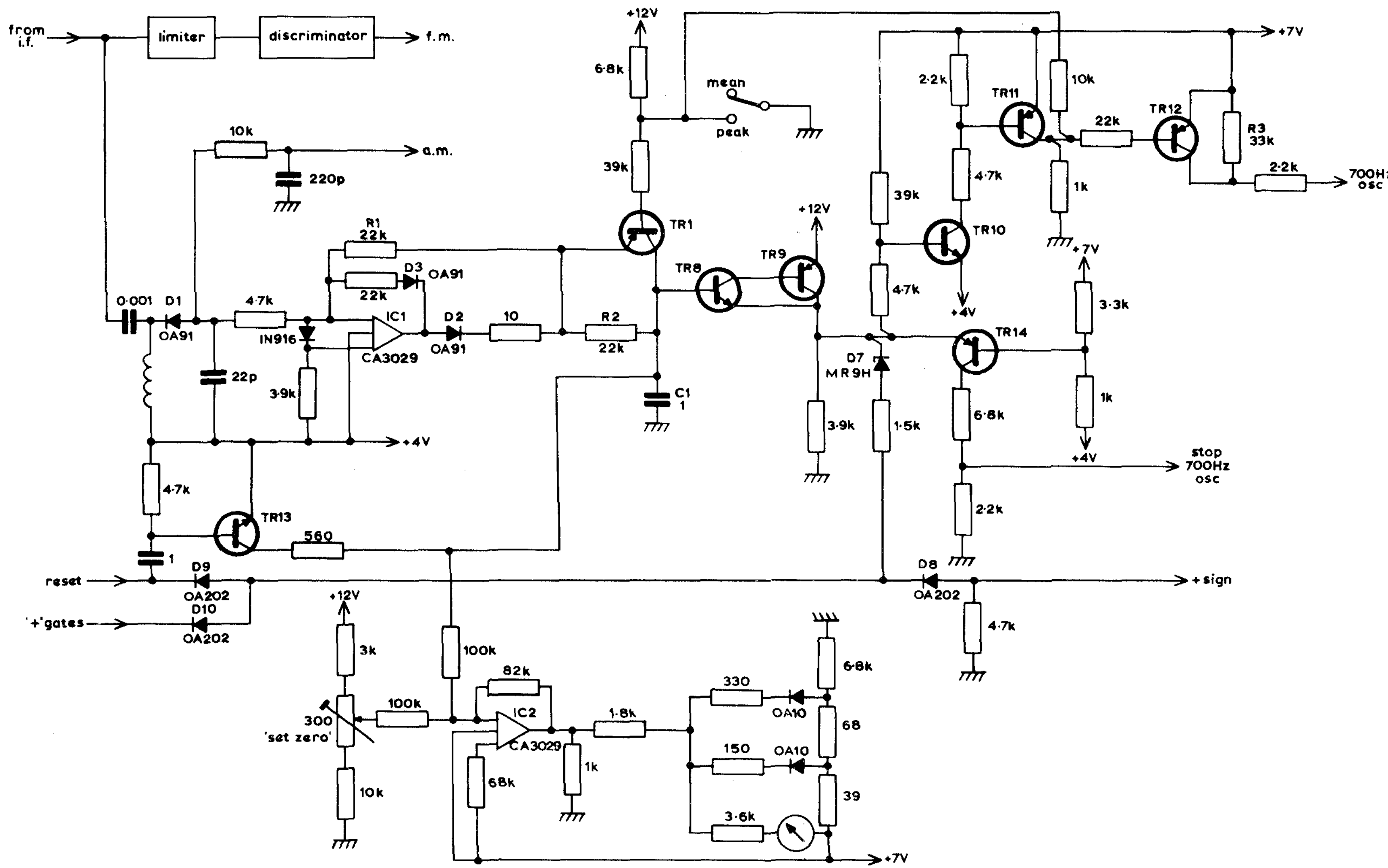

Fig. 6 - Detector and metering circuit diagram

count oscillator does not run. The coincidence gates of IC 2 will also detect this condition and, with the diode logic of D7 to D10, cause the + sign to be illuminated on the display. Hence a visual warning is given to the operator should an attempt be made to measure signals outside the range of the receiver.

5.3. The Display Counter and Associated Logic

The object of the display counter is to count the number of 0·2 dB attenuator steps which have been removed from the i.f. amplifier in order to achieve standard output from the detector, and to decode and display the result on neon numeral tubes.

The counter consists of three groups, the first contains three JK flipflops arranged as a divide-by-five unit.[5] The second group, as shown in Fig. 8, comprises a single JK flipflop followed by a second divide-by-five unit. The third consists of four JK flipflops. With the exception of the final flipflop each individual stage has a separate input from the decade switch in addition to its normal feed so that each stage can be set to a predetermined value by the decade switch for the conversion of input terminal voltage to field strength.

At the start of a cycle all the flipflops are reset by the pulse from the rate oscillator; this is followed after about 2 μ secs by pulses from the decade switch to individual counter stages setting each one into the required starting condition. Further pulses are then fed into the first stage of the counter from the 700 Hz oscillator which is controlling the i.f. attenuator steps. Thus, the display counter keeps a record of the attenuator condition.

Each display counter stage is connected to a corresponding store which only changes state when it receives a delayed trigger pulse at the end of each count period from the bistable IC 6 (Fig. 7) in the i.f. unit. Once the stores have been set, the new value is held until the next count has been completed.

The outputs from the stores are decoded to form the drives for the display tubes. The decoding is arranged so that the numerical display decreases with an increasing count.

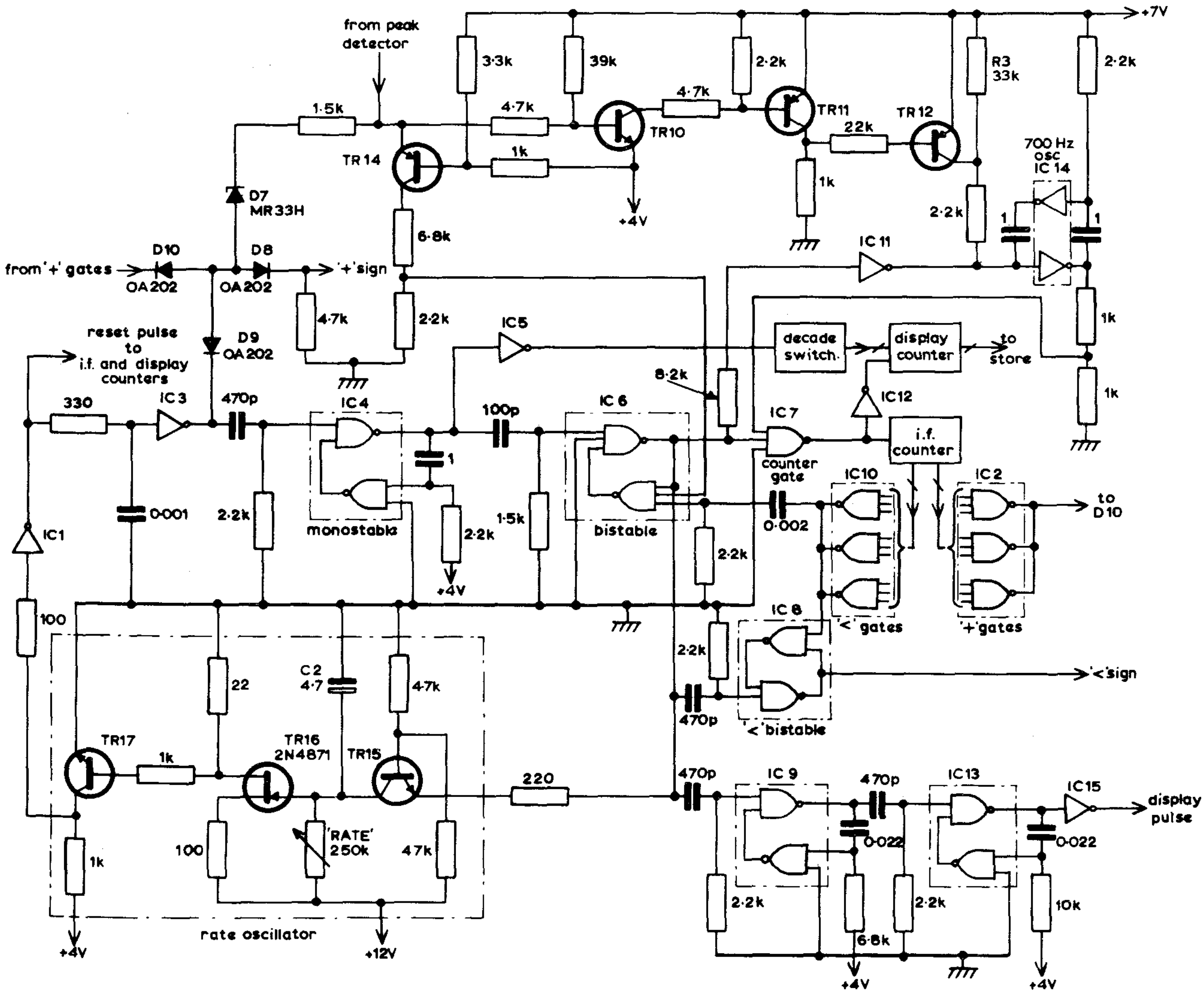

Fig. 7 - I.F. logic and limit circuit diagram

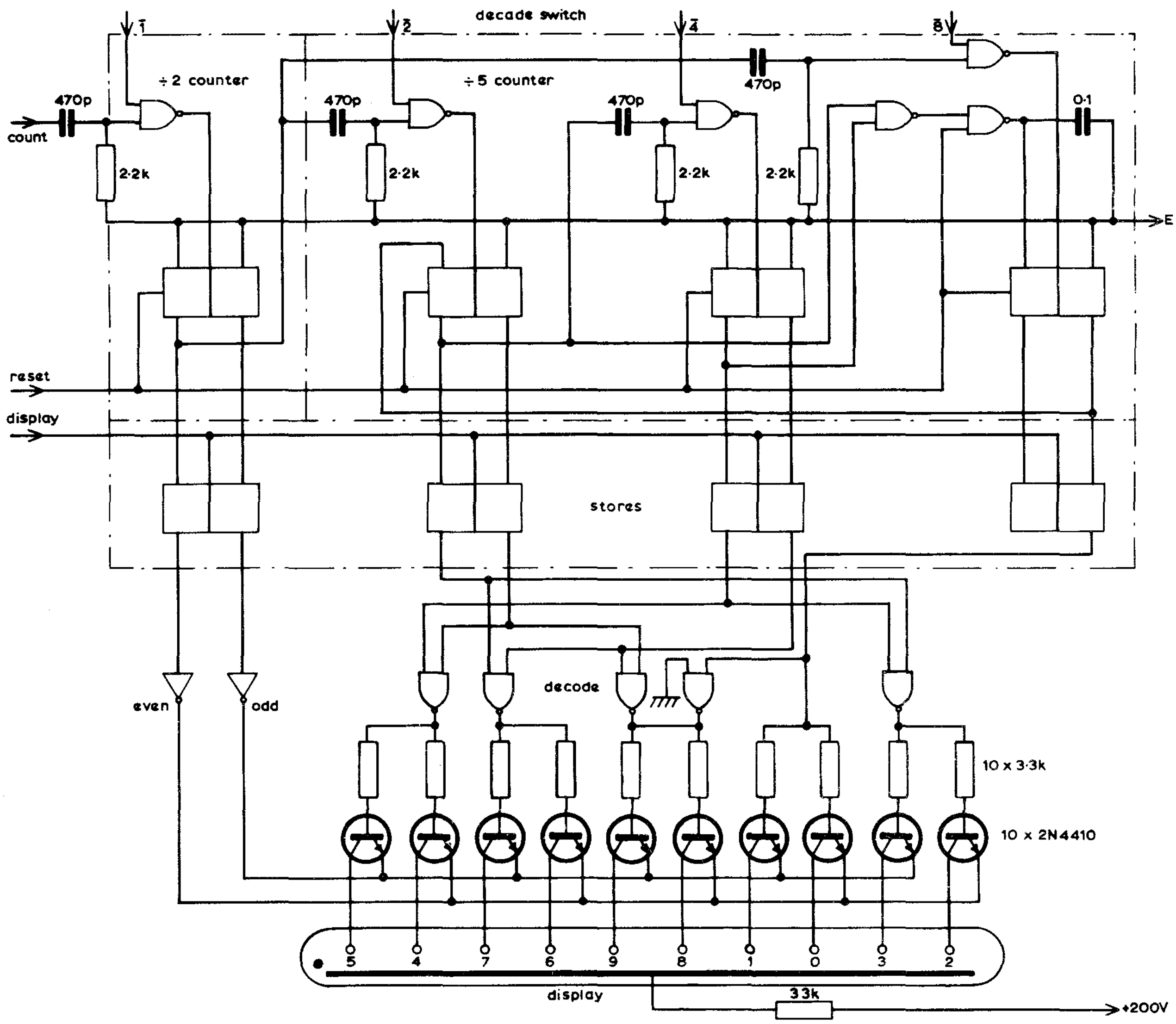

Fig. 8 - Units display counter and associated decoding

The display consists of a character tube, three neon numeral tubes and a decimal point together with transistor drivers. The character tube is used for the various signs and the hundred indication. The tens and units numeral tubes each have their drive transistors split into odd and even groups. Fig. 8 shows the circuit arrangement for the units display. The emitters of the drive transistors are then driven by either the odd or the even store output, whilst the bases are driven in pairs by the decoding gates. This arrangement simplifies the decoding and reduces the number of gates required. The final numeral tube giving the fractions of a decibel employs five drive transistors with a common emitter load, since only even digits are displayed.

5.4. The Rate Oscillator

The rate oscillator consists of a unijunction relaxation oscillator TR16 and is shown in Fig. 7. It is triggered by the display pulse from the bistable IC 6 in the i.f. amplifier logic. This pulse releases the clamp TR15 on the timing capacitor C2 from earth, and allows the capacitor to charge towards +12 V at a rate depending on the setting of the RATE control. When the potential across the capacitor reaches about 8 V the unijunction fires and discharges the capacitor producing a pulse which resets all the counter stages ready for another measurement.

5.5. The Audio Amplifier

The audio amplifier is fed via a volume control from either the a.m. or f.m. detector. It consists of an eight lead dual-in-line plastic package feeding a 25 Ω loudspeaker.

5.6. The Power Supplies

The receiver requires power supplies of 4 V, 7 V, 12 V and 200 V. These are derived from either a vehicle 12 V battery with negative earth or from 200 to 250 V, 50 Hz mains.

The three low voltages are stabilized using an integrated circuit voltage regulator. Short-circuit

current limiting is built into the regulator. The 200 V supply, used for the indicator tubes and noise diode is obtained from an inverter operating at 17 kHz. A voltage doubler is used for rectification and this is followed by a single stage of stabilization. A small boost voltage from the inverter is used to ensure that the 12 V stabilized line is maintained over a battery voltage range of 10 V to 17 V. A safety diode is incorporated in the battery lead to prevent damage should the receiver be inadvertently connected to a supply of wrong polarity.

On mains the supply is transformed and rectified to 13 V to replace the external battery.

The power requirements are approximately 30 W at 12 V.

6. CONCLUSIONS

A field strength measuring receiver for u.h.f. television transmissions has been described. The numeric display (in decibels above 1 μV/m) is considered easy to read and less liable to operator error than the normal system whereby a meter has to be read, added to an attenuator reading and further corrected by an aerial-calibration constant before obtaining the field strength.

The method of obtaining the logarithmic law is novel and, as it depends only on resistance values, should be stable and relatively easy to set up.

It is too early to express final conclusions on the behaviour of the receiver in the field but from the limited trials so far carried out the receiver is expected to give a satisfactory performance.

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